A GaAs Monolithic 6 GHz Low-Noise Amplifier for Satellite Receivers

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Abstract—**A design approach and accurate modeling techniques have been developed to realize a GaAs monolithic, 6 GHz, two-stage, low-noise amplifier (LNA) with a measured 1.7 dB noise figure and associated 21 dB gain. This self-biased LNA design, with chip dimensions of 80×135 mil, utilizes an ion-implantation FET model which predicts measured in-band amplifier gain to within 0.5 dB and peak frequency response to within 4 percent. The derived noise parameter estimation process, which uses a Gaussian elimination technique to predict the measured noise figure to within 0.2 dB, reduces a set of complex binomial equations to simple relationships which are easily programmable. A deep-recessed gate realization of this LNA design demonstrates that LNA low-noise performance is achievable under FET saturated drain current conditions.**

I. Introduction

SUCCESSFUL realization of monolithic microwave integrated circuitry (MMIC) requires accurate FET and circuit models, practical circuit design choices, and reproducible fabrication process steps. These elements have been combined to develop a GaAs MMIC 6 GHz, two-stage FET low-noise amplifier (LNA). Future satellite systems will benefit from the increased reliability and reduced cost provided by similar MMIC applications [1]–[3].

GaAs MMIC reproducibility is dependent on the method of wafer active layer generation used. Active layer uniformity is of particular importance for multistage stagger-tuned design applications such as two-stage LNA's. Ion implantation, which has an important advantage over liquid or vapor-phase epitaxy by producing better across-wafer uniformity, is, therefore, the preferred choice for MMIC LNA realization. Correct FET noise parameter characterization is also an essential element of a successful LNA design.

This paper describes an easily implemented noise parameter estimation process which predicts from simple microwave measurements the FET (minimum noise) source impedance required to complete an LNA design. The resulting MMIC LNA realization and fabrication techniques are also described, with particular emphasis on the effects of deep-recessed FET gates on LNA low-noise performance of saturated drain current.

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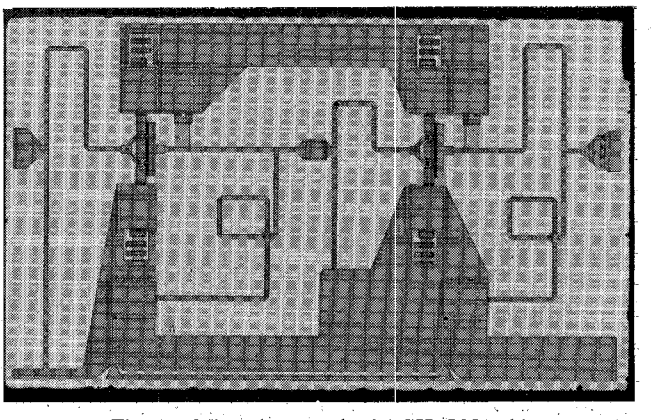

Fig. 1. Microphotograph of 6 GHz LNA chip.

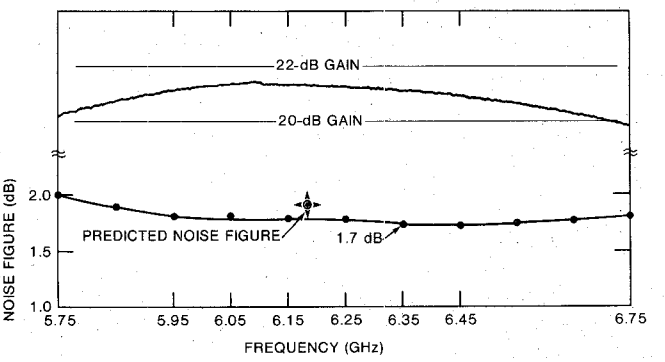

Fig. 2. LNA measured response.

II. Microstrip LNA Realization

The microstrip realization shown in Fig. 1 uses an ion-implantation process to fabricate the 0.5 μm×300 μm FET's and resistors. The FET model is computed from a known ion-implantation profile, peak doping density, and gate recess depth selected for low noise. This LNA design produces 21 dB of gain and better than 17 dB of output return loss over the 500 MHz *C*-band satellite bandwidth, with a noise figure of less than 2 dB over a 2 GHz bandwidth, as shown in Fig. 2. Measured 1 dB gain-compressed output power is +12 dBm. The in-band measured minimum noise figure of 1.7 dB closely matches the value predicted by a COMSAT-developed mathematical routine for the solution of the FET noise parameters, and approaches the state of the art for ion-implanted GaAs FET

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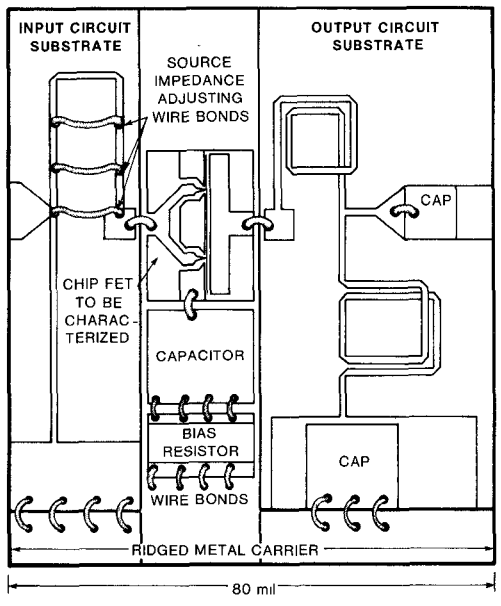

Fig. 3. Noise parameter estimation data collection amplifier.

amplifier technology. The successful LNA design is predicated on the LNA input circuit (source impedance) as defined by these noise parameters.

III. Noise Parameter Estimation Process

The linear two-port noise parameter estimation process requires only four sets of amplifier measurements at the frequency of interest, and regards the FET as a "black box." Other estimation techniques described in the literature [4], [5] use larger sets of measurement data to enhance the prediction accuracy. However, these techniques use involved computer-aided iterative routines for the solution of the large set of simultaneous equations. By contrast, the derived noise parameter estimation process used for this LNA design can be performed with a simple hand-held calculator.

Accuracy of the required four sets of amplifier measurements has been maintained through the use of input circuitry which is easy to adjust and measure or model. By utilizing removable input circuit wire bonds, these measurements can be made quickly and without the use of error-inducing tuners.

As shown in Fig. 3, a simple (nonoptimum LNA) MIC microstrip FET amplifier circuit is used to collect the estimation data. The FET to be characterized is ridge-mounted on a metal carrier which contains separate substrates of GaAs input and output circuits. The carrier fits into a metal package, housing SMA coaxial input and output connectors which are gold-ribbon bonded to the microstrip circuit at the carrier-to-package interface. The package design is common to both the MIC test and MMIC LNA amplifiers and therefore allows package transmission attenuation to be removed from the estimation data. The use of 1-mil-wide input circuit transmission lines and wire bonds of similar width in the ladder structure, shown in Fig. 3, produces adjustable source impedances which can be accurately modeled, using a microwave circuit analysis computer program, or measured on a network analyzer. Through the estimation process, the measurements produce both the FET optimum design source impedance and the minimum noise figure prediction. Correlation between the predicted and measured minimum noise figures at 6 GHz for several LNA designs has been within 0.2 dB.

A brief development of this noise parameter estimation process begins from a wave description of the relationship between the linear two-port noise figure and the signal source reflection coefficient [6], [7], as

$$F_x = F_{\mathrm{MIN}} + 4(R_N/Z_0)\left[\frac{|\Gamma_{sx} - \Gamma_{on}|^2}{(1-|\Gamma_{sx}|^2)|1+\Gamma_{on}|^2}\right]$$

where

F_{MIN} = minimum (optimum) noise figure of the linear two-port,
R_N = equivalent noise resistance of the linear two-port, expressed in Ω,
Z_0 = characteristic impedance of the measurement system,
Z_{sx} = arbitrary signal source impedance,
Γ_{sx} = arbitrary source reflection coefficient $= (Z_{sx} - Z_0)/(Z_{sx} + Z_0)$,
Γ_{on} = optimum noise figure source reflection coefficient,
F_x = noise figure associated with Z_{sx},
$R_N/Z_0 = r_N$ = normalized noise resistance.

Therefore, the noise characteristics of any linear two-port are completely defined at a particular frequency by the following set of four noise parameters: $[F_{\mathrm{MIN}}, R_N, \mathrm{Re}(\Gamma_{on}), \mathrm{Im}(\Gamma_{on})]$. Consequently, the noisy linear two-port can be considered as a black box whose noise parameters can be mathematically extracted using the above relationship and four independent non-zero-producing (nonsingular) sets of simple microwave measurements (F_x, Γ_{sx}) at the frequency of interest [4]. A linear two-port equivalent circuit is therefore not required.

The linear two-port noise parameters are determined by applying a Gaussian elimination technique [8] to a set of simultaneous complex binomial equations derived from the above relationship. This wave relationship can be expressed as

$$F_{\mathrm{MIN}} = F_x - 4r_N\Delta_x$$

where

$$\Delta_x = \frac{|\Gamma_{sx} - \Gamma_{on}|^2}{\Phi_x|1+\Gamma_{on}|^2}$$

and

$$\Phi_x = \left[1 - |\Gamma_{sx}|^2\right].$$

Because four sets of measurements are required ($X = 1,2,3,4$), a set of simultaneous second-order equations is

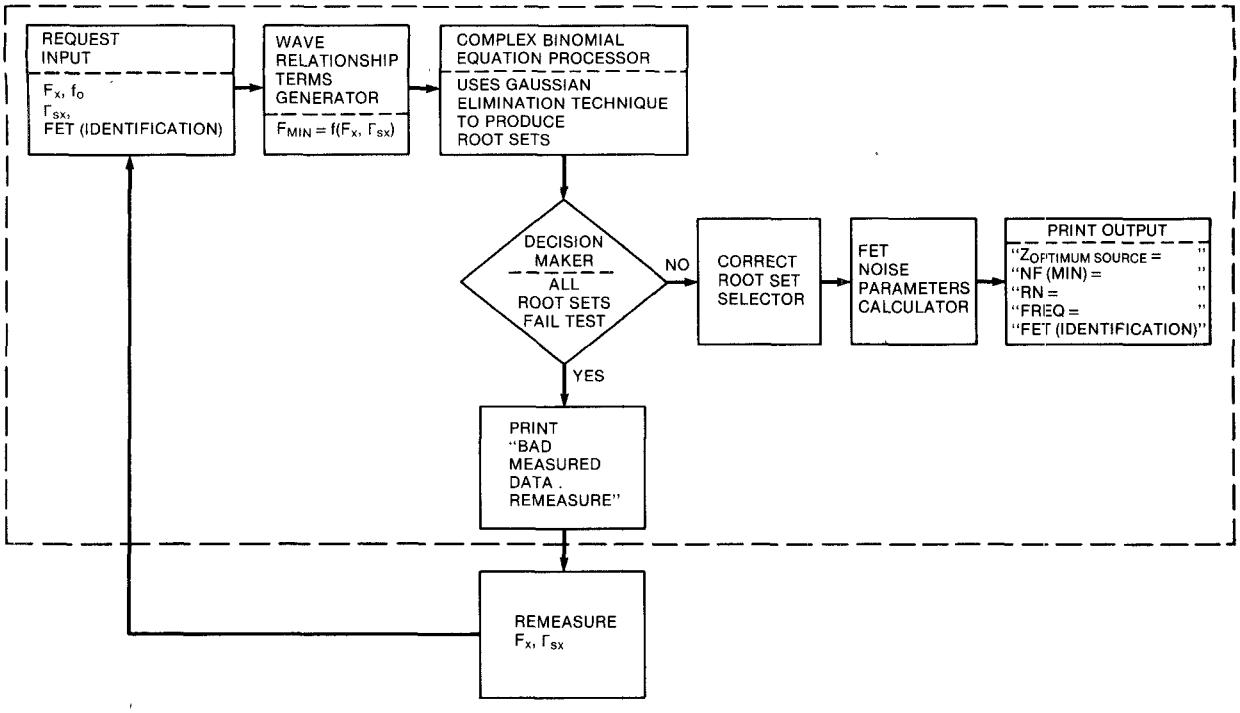

Fig. 4. QUIETFET noise parameter estimation process.

produced. Relating these equations in pairs and letting $(F_2 - F_1) = \gamma$ and $(F_4 - F_3) = \beta$ results in

$$\gamma(\Delta_4 - \Delta_3) = \beta(\Delta_2 - \Delta_1).$$

Letting $\Gamma_{sx} = A_x + jB_x$, expanding the Δ_x function, and substituting yields

$$\begin{aligned}
&\gamma\Phi_1\Phi_2\Phi_3\left[(A_4 - A)^2 + (B_4 - B)^2\right] \\
&\quad - \gamma\Phi_1\Phi_2\Phi_4\left[(A_3 - A)^2 + (B_3 - B)^2\right] \\
&\quad = \beta\Phi_1\Phi_3\Phi_4\left[(A_2 - A)^2 + (B_2 - B)^2\right] \\
&\quad - \beta\Phi_2\Phi_3\Phi_4\left[(A_1 - A)^2 + (B_1 - B)^2\right].
\end{aligned}$$

Letting

$$\begin{aligned}
K &= \gamma\Phi_1\Phi_2\Phi_3 \\
L &= \gamma\Phi_1\Phi_2\Phi_4 \\
M &= \beta\Phi_1\Phi_3\Phi_4 \\
N &= \beta\Phi_2\Phi_3\Phi_4
\end{aligned}$$

expanding, forming one homogeneous equation, and separating real and imaginary terms results in separate quadratic equations for A and B, whose solutions take the form

$$A(\text{or } B) = \left[-b \pm \sqrt{b^2 - 4ac}\right]/2a$$

where for A,

$$\begin{aligned}
a &= (K - L - M + N) \\
b &= -2(KA_4 - LA_3 - MA_2 + NA_1) \\
c &= \left(KA_4^2 - LA_3^2 - MA_2^2 + NA_1^2\right)
\end{aligned}$$

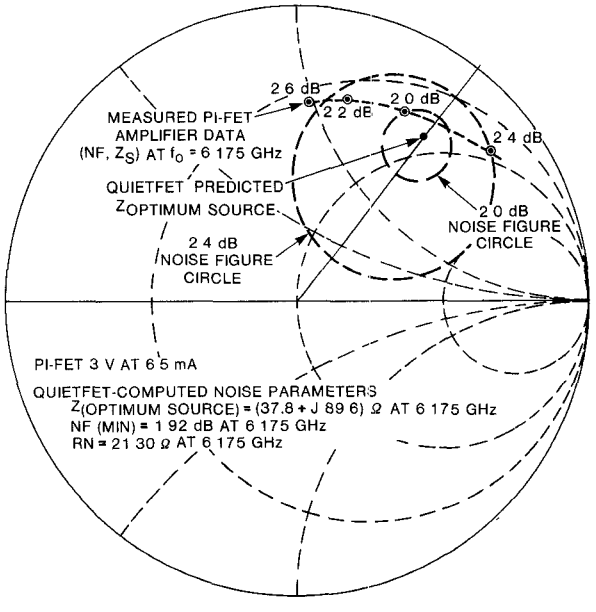

Fig. 5. Smith chart representation of QUIETFET predicted PI-FET Z (optimum, source) at 6.175 GHz.

and for B,

$$\begin{aligned}
a &= (K - L - M + N) \\
b &= -2(KB_4 - LB_3 - MB_2 + NB_1) \\
c &= \left(KB_4^2 - LB_3^2 - MB_2^2 + NB_1^2\right).
\end{aligned}$$

The correct set of roots for A and B is chosen from critical attributes, and the two-port noise parameters are now completely determined for the frequency of interest.

A correct selection of roots is accomplished by iteratively testing all roots sets using the F_{MIN} relationship. The correct set produces the lowest positive F_{MIN} value. This

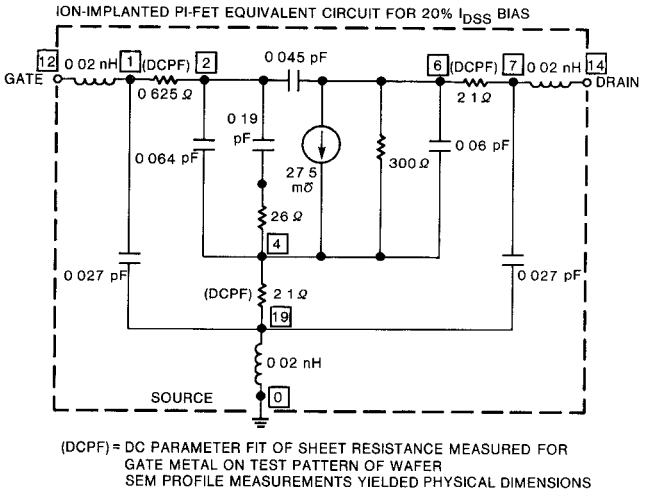

Fig. 6. Ion-implanted PI-FET equivalent circuit.

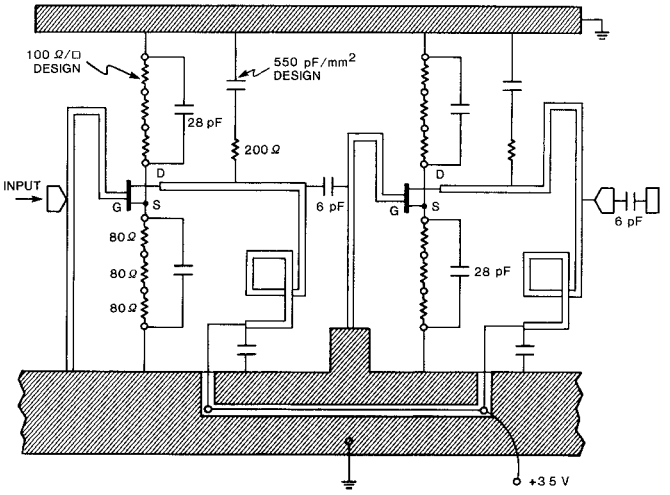

Fig. 7. LNA coupled-line distributed element circuit model.

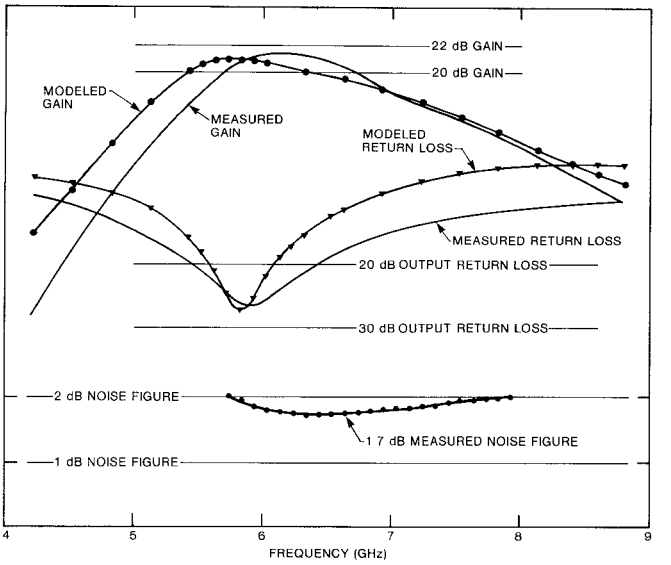

Fig. 8. LNA measured versus modeled response.

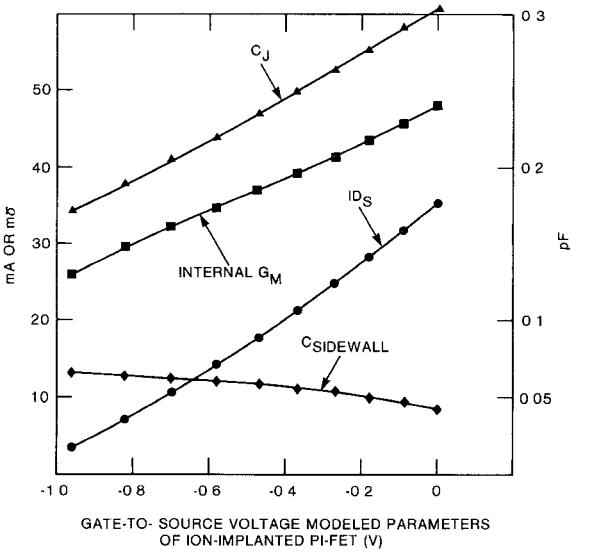

Fig. 9. Modeled PI-FET parameter dependence on gate-to-source voltage.

set is then used to calculate an average value of F_{MIN} based on the four sets of original measured data.

A user-friendly Fortran computer program, QUIET-FET, has been written to handle this mathematical routine. It prompts the user for noise figure data in decibels and source impedances in ohms, performs the necessary calculations, and prints the computed noise parameters. Fig. 4 shows the noise parameter estimation process in block diagram form. Fig. 5 shows the Smith chart representation of the four sets of measured data used to calculate the estimated FET noise parameters also shown in QUIET-FET output format.

IV. Gain Estimation Process

A low-noise-biased equivalent circuit of the COMSAT-developed 0.5 μm$\times$300 μm FET (named PI-FET for its physical appearance) has been created as a design aid for gain and output return loss prediction [9]. The equivalent circuit parameters are derived from an in-house-created modeling system of computer programs for the simulation of GaAs FET performance. The modeling system, which accounts for FET device physics, uses input parameters which relate closely to the fabrication process. Examples of these input parameters are peak carrier concentration, carrier profile shape, and gate recess depth. The resulting PI-FET equivalent circuit, shown in Fig. 6, together with the LNA coupled-line distributed-element circuit model shown in Fig. 7, provides precise modeling, predicting in-band gain and output maximum return loss responses to within 0.5 dB and peak frequency response to within 4 percent, as shown in Fig. 8. The computer system modeled dependence of PI-FET parameters on gate-to-source voltage is shown in Fig. 9.

V. LNA Design Approach

The successful design of an MMIC LNA is dependent on the combination of accurate circuit and FET modeling within the MMIC circuit layout constraints, and on reproducible fabrication process steps brought together to meet

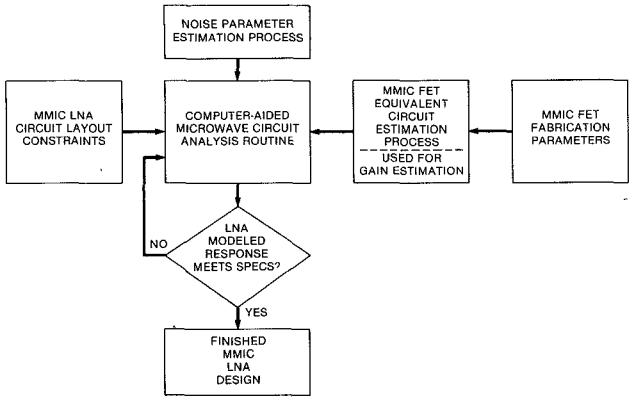

Fig. 10. MMIC LNA design procedure.

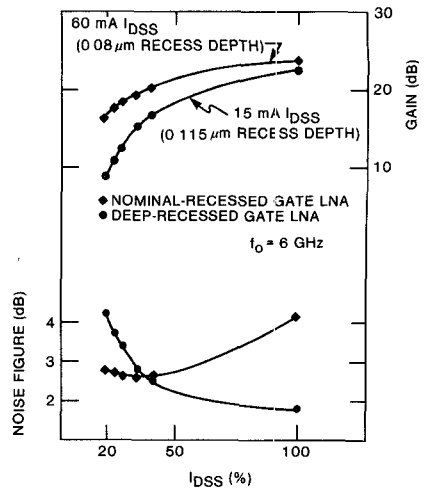

Fig. 11. LNA noise figure and gain dependence on drain current as a function of gate recess depth.

the application requirements. The design procedure, shown in Fig. 10 in flowchart form, uses noise parameter and FET equivalent circuit estimation processes to drive the microwave circuit design toward an acceptable modeled LNA response.

The two-stage MMIC 6 GHz LNA is a self-biased design with grounded gates to protect the FET's from voltage transients. As such, the circuit requires only one bias voltage (3.5 V). Ion-implanted 80 Ω bias resistors are series-stacked, with wire-bondable taps for drain current adjustment.

The first-stage design is fixed for minimum noise figure at the expense of gain slope. The input circuit (source impedance) is fixed at 6.175 GHz by the noise parameter estimation process described above. The second-stage design is a trade-off of noise figure for two-stage gain slope equalization. Both stages use self-inductive coupled spiral lines to reduce physical line lengths. In an effort to maintain straightforward circuit models of the elements used in this two-stage design, overcrowding of the distributed lines was avoided, resulting in the predictable minimum noise figure and gain response. Overall GaAs MMIC circuit size is $80 \times 135 \times 12.5$ mil.

VI. Circuit Fabrication Process Detail

A dual selective ion implantation process was used to create an N peak carrier concentration of 2.7×10^{17} cm^{-3} only in the FET channel areas, and an ($N+N^+$) implant sheet resistivity, ρ, of 100 Ω/square only in the MMIC resistor areas. The gate recess depth was etched for low-noise operation, and then the 0.5 μm gates were E-beam written. Compact RF bypass and dc-blocking capacitors use silicon nitride dielectric of 0.1 μm thickness to achieve 550 pF/mm^2. Coupled transmission lines of 1 mil width and spacing utilize dielectric-protected air bridges.

The channel was formed by a 100 keV silicon implant and the N^+ layer for device ohmic contacts was formed by a 200 keV silicon implant with peak carrier density of approximately 1×10^{18}/cm^3. The implanted resistors were fabricated in the same steps as the contact areas. The ohmic contacts were alloyed Au/Ge/Ag/Au. The gates were Ti/Pt/Au. The gate metal also formed the bottom plates of the capacitors. The FET's were designed with two parallel gate feeds. A 2 μm plated gold layer formed the inductors, the top plates of the capacitors, the overlay metal on ohmic contacts, and other passive circuit element areas. Plated gold air bridges were used to interconnect the FET sources, to contact the top plates of capacitors, and to connect the crossovers for the spiral inductors.

VII. Effect of FET Gate Recess Depth on LNA Noise Figure

Because of the dependence of FET noise figure on diffusion noise, source resistance, drain current, and transconductance (G_m), and the direct relationship between G_m and drain current, an optimum deep recess depth for the 0.5 μm gate exists for a low-noise-optimized ion-implantation profile in which FET low-noise operation can be achieved at saturated drain current [10], [11]. These conditions were attained for one deeply recessed wafer of this LNA design in which a low I_{dss} of 15 mA was achieved. The computer-generated FET performance simulation indicates that the corresponding depth is 44 percent over nominal. The low I_{dss} and high associated G_m produced a good noise figure of 1.9 dB and a gain of 23 dB at 6 GHz. The weak dependence of LNA noise figure on drain current (shown in Fig. 11) is probably attributable to reduced diffusion noise and recess-enhanced G_m associated with the deeply recessed gate region [10], [12], [13]. The effect of gate recess depth variation on LNA noise figure and gain is also shown in Fig. 11.

VIII. Summary

A GaAs monolithic 6 GHz, two-stage LNA design has been realized by using accurate modeling techniques to obtain a measured 1.7 dB noise figure and associated 21 dB gain. The MMIC circuit size is $80 \times 135 \times 12.5$ mil.

The derived noise parameter estimation process, which is easily programmable, predicts the measured noise figure to within 0.2 dB. The gain estimation process, which accounts for the FET ion-implantation profile, peak carrier concentration, gate recess depth, resistor sheet ρ, and

microwave distributed circuitry, predicts the in-band gain response to within 0.5 dB.

A deep-recessed gate realization of this LNA design has demonstrated that LNA low-noise performance can be achieved for FET saturated drain current conditions because of associated FET reduced diffusion noise and recess-enhanced transconductance.

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REFERENCES

[1] C. Mahle and H. Huang, "MMIC's in communications," *IEEE Communications Magazine*, vol. 23, pp. 8–16, Sept. 1985.

[2] J. Potukuchi, B. Geller, R. Mott, and R. Gupta, "Design and development of monolithic 6/4-GHz transponder subsystem," in *Proc. Government Microcircuit Applications Conference (GOMAC)* (Orlando, FL), Nov. 5–7, 1985, pp. 353–354.

[3] R. Gupta, J. Reynolds, M. Fu, and T. Heikkila, "Design and modeling of a GaAs monolithic 2- to 6-GHz feedback amplifier," *COMSAT Tech. Rev.*, to be published.

[4] R. Q. Lane, "The determination of device noise parameters," *Proc. IEEE*, vol. 57, pp. 1461–1462, Aug. 1969.

[5] M. Sannino, "On the determination of device noise and gain parameters," *Proc. IEEE*, vol. 67, pp. 1364–1366, Sept. 1979.

[6] R. P. Meys, "A wave approach to the noise properties of linear microwave devices," *IEEE Trans. Microwave Theory Tech.*, vol. MTT-26, pp. 34–37, Jan. 1978.

[7] C. A. Liechti, "Microwave field-effect transistors—1976," *IEEE Trans. Microwave Theory Tech.*, vol. MTT-24, pp. 279–300, June 1976.

[8] F. Scheid, *Theory And Problems of Numerical Analysis*. New York: McGraw-Hill, 1968, pp. 334–340.

[9] T. Smith, "A modeling system for simulation of GaAs FET performance," *COMSAT Tech. Rev.*, vol. 15, no. 2, pp. 237–258, Fall 1985.

[10] K. Ohata, H. Itoh, F. Hasegawa, and Y. Fujiki, "Super low-noise GaAs MESFET's with a deep-recess structure," *IEEE Trans. Electron Devices*, vol. ED-27, pp. 1029–1034, June 1980.

[11] M. Ogawa, K. Ohata, T. Furutsuka, and N. Kawamura, "Submicron single-gate and dual-gate GaAs MESFET's with improved low noise and high gain performance," *IEEE Trans. Microwave Theory Tech.*, vol. MTT-24, pp. 300–305, June 1976.

[12] R. A. Pucel, D. J. Masse, and C. F. Krumm, "Noise performance of gallium arsenide field-effect transistors," *IEEE J. Solid-State Circuits*, vol. SC-11, pp. 243–255, Apr. 1976.

[13] R. W. H. Engelmann and C. A. Liechti, "Gunn domain formation in the saturated current region of GaAs MESFET's," in *Dig. Int. Electron Devices Meeting*, 1976, pp. 351–354.

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